

WHAT IS CLAIMED IS:

1. A system for providing oscillator control throughout a first operating range, said system comprising:

a controllable oscillator;

5 a phase lock loop circuit coupled to said controllable oscillator, wherein said phase lock loop circuit has a second operating range, wherein said second operating range is selected independent of a desired width of said first operating range to provide an acceptable level of operational characteristics; and

10 a control circuit coupled to said controllable oscillator, wherein said control circuit provides a control signal to said controllable oscillator to selectively adjust said second operating range to correspond to a desired portion of said first operating range.

2. The system of claim 1, wherein said controllable oscillator comprises:

a voltage controlled oscillator having an aging specification substantially greater than that of a precision OCXO.

3. The system of claim 1, wherein said phase lock loop circuit comprises:

a digital phase lock loop circuit; and

5 a digital to analogue convertor, wherein said digital to analogue convertor accepts digital oscillator control information from said digital phase lock loop circuit and provides an analogue control signal for use in controlling said controllable oscillator.

4. The system of claim 3; wherein said digital to analogue convertor is a high resolution digital to analogue convertor.

5. The system of claim 4, wherein said high resolution digital to analogue convertor is selected from the range from a 10 bit analogue converter to a 16 bit analogue converter.

6. The system of claim 3, wherein provision of an analogue control signal for use in controlling said controllable oscillator by said digital to analogue converter includes utilization of most significant bit information from said control circuit in combination with accepting least significant bit information from said digital phase lock loop circuit.

7. The system of claim 3, further comprising:
a multiplexer circuit disposed in the signal path between said digital phase lock loop circuit and said digital to analogue convertor, wherein said multiplexer circuit is also disposed in a signal path between said control circuit and said digital to analogue convertor.

8. The system of claim 7, wherein said control circuit provides a control signal through said multiplexer circuit to select said desired portion of said first operating range to which said second operating range corresponds.

9. The system of claim 3, further comprising:
a buffering circuit coupled to said digital to analogue convertor.

10. The system of claim 9, wherein said buffering circuit provides hysteresis control of operation of said controllable oscillator.

11. The system of claim 9, wherein said buffering circuit latches most significant bit oscillator control information from said control circuit for use with variable least significant bit oscillator control information from said phase lock loop circuit.

12. The system of claim 1, further comprising:
a memory coupled to said control circuit.

13. The system of claim 12, wherein said memory stores historical oscillator control information.

14. The system of claim 13, wherein said historical oscillator control information is information with respect to a portion of said first operating range said second operating range has recently successfully operated within.

15. The system of claim 13, wherein said historical oscillator control information is information with respect to a rate at which control of said oscillator is changing over time.

16. The system of claim 1, wherein said control circuit comprises:
a processor operating under control of an algorithm; and

a sweep algorithm operable on said processor, wherein said sweep algorithm selects various desired portions of said first operating range for which to adjust said second operating range to correspond to acquire synchronization of said oscillator with a master oscillator.

17. The system of claim 16, wherein said various desired portions are selected for adjustment of said second operating range in a pattern determined to acquire said synchronization efficiently.

18. The system of claim 17, wherein said pattern is incremental adjustment to substantially fully scan a particular substantially contiguous portion of said first range.

19. The system of claim 18, wherein said incremental adjustment is interleaved to cover a portion of said first range below a nominal position and a portion of said first range above a nominal position.

20. The system of claim 18, wherein said incremental adjustment is in a direction from a nominal position which historical information regarding control of said oscillator indicates synchronization is most likely to be achieved.

21. The system of claim 17, wherein said pattern is spotted adjustment to selectively scan noncontiguous portions of said first range.

22. The system of claim 1, wherein said first operating range is selected to accommodate component operational drift associated with an extended system operational life.

23. The system of claim 1, further comprising:

a signal comparison circuit coupled to said control circuit, wherein said signal comparison circuit provides said control circuit with information when a data match is identified in a recovered signal.

24. A method for providing oscillator synchronization, said method comprising the steps of:

operating a controllable first oscillator in a phase lock loop mode of operation, wherein a frequency of said first oscillator is synchronized with a frequency of a second oscillator over a first range of frequencies less than a second range of frequencies over which synchronization is desired;

detecting when operation in said phase lock loop mode of operation is unable to maintain synchronization of said first oscillator with said second oscillator; and

operating in a sweep mode of operation when said detecting step indicates said phase lock loop mode of operation is unable to maintain synchronization of said first oscillator with said second oscillator, wherein said sweep mode of operation comprises the steps of:

providing control signals to adjust said first range of frequencies with respect to said second range of frequencies, wherein adjustment of said first range of frequencies causes said first range of frequencies to correspond to a different portion of said second range of frequencies without broadening said first range of frequencies; and

detecting if said phase lock loop mode of operation is able to acquire synchronization of said first oscillator with said second oscillator, wherein said providing range adjusting control signals step is repeated if it is determined said phase lock loop mode of operation is not able to acquire synchronization of said first oscillator with said second oscillator.

25. The method of claim 24, wherein said operating a controllable first oscillator step comprises the step of:

operating a digital phase lock loop circuit to provide a digital oscillator control signal to a high resolution digital to analogue convertor.

26. The method of claim 25, further comprising the step of:

providing a digital oscillator control signal to said high resolution digital to analogue convertor from a controller, wherein said digital oscillator control signal from said operating a digital phase lock loop circuit step and said digital oscillator control signal from said controller are both at least in part utilized to establish a position said second range said phase lock loop mode of operation is operated within at said operating a controllable first oscillator step.

27. The method of claim 24, wherein said detecting synchronization step comprises the step of:

comparing a recovered timing signal associated with said second oscillator to a clock signal associated with said first oscillator.

28. The method of claim 24, wherein said detecting synchronization step comprises the steps of:

monitoring information with respect to control of said first oscillator over a preselected period of time; and

determining if more than an acceptable number of oscillator control changes have occurred within the preselected period of time.

29. The method of claim 24, wherein said detecting if said phase lock loop mode of operation is able to acquire synchronization comprises the step of:

comparing a recovered data signal with a known data pattern to determine if a matching data pattern has been recovered.

30. The method of claim 24, wherein said sweep mode of operation step further comprises the step of:

determining a beginning portion of said second range of frequencies to adjust said first range of frequencies most likely to allow said phase lock loop mode of operation to acquire synchronization of said first oscillator with said second oscillator.

31. The method of claim 30, wherein said determining step comprises the step of:

identifying a portion of said second range of frequencies said phase lock loop mode of operation has recently acquired synchronization of said first oscillator with said second oscillator.

32. The method of claim 30, wherein said sweep mode of operation step further comprises the step of:

selecting subsequent portions of said second range of frequencies to adjust said first range of frequencies based at least in part on information with respect to historical change of control of said first oscillator.

33. The method of claim 32, wherein said historical change of control information is a direction of change of said first oscillator.

34. The method of claim 24, further comprising the step of:

monitoring information with respect to control of said first oscillator.

35. The method of claim 34, further comprising the step of:
storing at least a portion of said monitored information.

36 The method of claim 34, herein said monitored information includes information with respect to a portion of said second range of frequencies said phase lock loop mode of operation has recently acquired synchronization of said first oscillator with said second oscillator.

37. The method of claim 36, wherein said step of monitoring said information with respect to a portion of said second range of frequencies said phase lock loop mode of operation has recently acquired synchronization of said first oscillator with said second oscillator comprises the step of:

5 calculating an average portion of said second range of frequencies said phase lock loop mode of operation has acquired synchronization of said first oscillator with said second oscillator over a predetermined time span.

38. The method of claim 36, wherein said step of monitoring said information with respect to a portion of said second range of frequencies said phase lock loop mode of operation has recently acquired synchronization of said first oscillator with said second oscillator comprises the step of:

5 identifying a mean portion of said second range of frequencies said phase lock loop mode of operation has acquired synchronization of said first oscillator with said second oscillator over a predetermined time span.

39. The method of claim 34, wherein said monitored information includes information with respect to a direction of change of control of said first oscillator.

40. The method of claim 34, wherein said monitored information includes information with respect to a speed of change of control of said first oscillator.

41. The method of claim 40, wherein said information with respect to a speed of change of control of said first oscillator is utilized to predict system malfunction.

42. The method of claim 24, wherein said first range of frequencies is selected to provide an acceptable phase noise level of a phase lock loop circuit utilized in said phase lock loop mode of operation.

43. The method of claim 42, wherein said second range of frequencies is selected to allow for extended operation of said phase lock loop circuit.

44. The method of claim 42, wherein said first oscillator is utilized in providing both intermediate frequency clock signals and high frequency clock signals, and wherein said acceptable phase noise level is acceptable at both said intermediate frequency and said high frequency.

45. An automatic frequency compensation system comprising:

a voltage controlled oscillator;

a high resolution digital to analogue converter coupled to said voltage controlled oscillator;

5 a digital phase lock loop circuit coupled to said digital to analogue convertor to provide oscillator control bits to said digital to analogue convertor to effectuate control of said voltage controlled oscillator, wherein said digital phase lock loop circuit provides said oscillator control bits in response to a monitored clock signal associated with an output of said voltage controlled oscillator; and

10 a control circuit coupled to said digital to analogue convertor to provide oscillator control bits to said digital to analogue convertor to effectuate control of said voltage controlled oscillator, wherein said control circuit provides said oscillator control bits in response to a determination that said digital phase lock loop circuit is not able to provide desired frequency compensation results with respect to said voltage controlled oscillator.

46. The system of claim 45, wherein said digital phase lock loop circuit provides a limited frequency compensation range selected to provide a desired phase noise ceiling.

47. The system of claim 46, wherein control of said oscillator by said control circuit provides operation of said oscillator in a broad frequency compensation range, wherein said limited frequency compensation range is stepped through various portions of said broad frequency range under control of said control circuit.

48. The system of claim 45, wherein said control circuit comprises:

a processor, wherein said processor monitors control of said voltage controlled oscillator.

49. The system of claim 48, wherein said control circuit further comprises:

a memory storage device coupled to said processor, wherein said memory storage device stores information with respect to control of said voltage controlled oscillator.

50. The system of claim 49, wherein said processor monitors voltage controlled oscillator control information to determine an operational point at which a desired level of frequency compensation is achieved and stores information associated with the point at which a desired level of frequency compensation is achieved in said memory storage device.

51. The system of claim 50, wherein said stored information includes an average of operational points at which a desired level of frequency compensation is achieved.

52. The system of claim 50, further comprising:

a pattern matching circuit coupled to said processor, wherein said pattern matching circuit accepts data recovered using a clock signal associated with said voltage controlled oscillator and compares the recovered data to a known data pattern to provide an indication of status of frequency compensation operation to said processor wherein said determination of an operational point at which a desired level of frequency compensation is achieved is made at least in part through reference to information provided by said pattern matching circuit.

53. An method of providing automatic frequency compensation comprising the steps of:

providing a phase lock loop mode of operation to maintain frequency lock over a selected first range of frequency drift;

5 providing a sweep mode of operation to step operation of said phase lock loop first range of frequency drift over a selected second range of frequency drift; and

monitoring at least one of said phase lock loop mode of operation and said sweep mode of operation to determine a portion of said second range of frequency drift said first range is successfully able to maintain said frequency lock.

54. The method of claim 53, further comprising the step of:

providing a controllable oscillator operable under control of said phase lock loop mode of operation and said sweep mode of operation, wherein said phase lock loop mode of operation utilizes a first control signal to control said oscillator and said sweep mode of
5 operation utilizes a second control signal to control said oscillator.

55. The method of claim 54, wherein said oscillator is a voltage controlled oscillator.

56. The method of claim 54, further comprising the step of:

multiplexing said first control signal and said second control signal to enable said sweep mode of operation to step said operation of said phase lock loop first range of frequency drift over said second range of frequency drift.

57. The method of claim 56, wherein said phase lock loop mode of operation is provided by a digital phase lock loop circuit.

58. The method of claim 57, wherein said step of multiplexing selectively passes bits of said first control signal to a digital to analogue convertor.

59. The method of claim 53, wherein said monitoring step comprises the step of:
determining an average portion of said second range said first range is successfully
able to maintain said frequency lock.

60. The method of claim 53, wherein said monitoring step comprises the steps of:
monitoring operation of said phase lock loop mode of operation over a preselected
period of time; and

determining if more than an acceptable number of control signal changes have
5 occurred within the preselected period of time.

61. The method of claim 53, further comprising the step of:
storing at least a portion of information provided by said step of monitoring